

Hardware Implementation of Solar based Boost to SEPIC Converter Fed Nine Level Inverter System

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ABSTRACT

Multi level inverters are widely used in high power applications because of low harmonic distortion. This paper deals with the simulation and implementation of PV based boost to SEPIC converter with multilevel inverter. The output of PV system is stepped up using boost to sepic converter and it is converted into AC using a multilevel inverter. The simulation and experimental results with the R load is presented in this paper. The FFT analysis is done and the THD values are compared. Boost to SEPIC converter is proposed to step up the voltage to the required value. The experimental results are compared with the simulation results. The results indicate that nine level inverter system has better performance than seven level inverter system.

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1. INTRODUCTION

The extensive use of fossil fuels has resulted in the global problem of greenhouse emissions. Moreover, as the supplies of fossil fuels are depleted in the future, they will become increasingly expensive. Thus, solar energy is becoming more important since it produces less pollution and the cost of fossil fuel energy is rising, while the cost of solar arrays is decreasing. In particular, small-capacity distributed power generation systems using solar energy may be widely used in residential applications in the near future [1], [2].

The power conversion interface is important to grid- connected solar power generation systems because it converts the DC power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the DC power to ac power [2]-[4]. Since the output voltage of a solar cell array is low, a DC-DC power converter is used in a small-capacity solar power generation system to boost the output voltage, so it can match the DC bus voltage of the inverter. The power conversion efficiency of the power conversion interface is important to insure that there is no waste of the energy generated by the solar cell array. The active devices and passive devices in the inverter produce a power loss. The power losses due to active devices include both conduction losses and switching losses [5]. Conduction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. A filter inductor is used to process the switching harmonics of an inverter, so the power loss is proportional to the amount of switching harmonics.

The voltage change in each switching operation for a multi-level inverter is reduced in order to improve its power conversion efficiency [6]-[15] and the switching stress of the active devices. The amount of switching harmonics is also attenuated, so the power loss caused by the filter inductor is also reduced.

Therefore, multilevel inverter technology has been the subject of much research over the past few years. In theory, multilevel inverters should be designed with higher voltage levels in order to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI).

Conventional multilevel inverter topologies include the diode-clamped [6]-[10], the flying-capacitor [11]-[13], and the cascade H-bridge [14]-[18] types. Diode-clamped and flying-capacitor multilevel inverters use capacitors to develop several voltage levels. But it is difficult to regulate the voltage of these capacitors. Since it is difficult to create an asymmetric voltage technology in both the diode-clamped and the flying-capacitor topologies, the power circuit is complicated by the increase in the voltage levels that is necessary for a multilevel inverter. For a single-phase seven-level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage [17], so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a DC bus voltage of multiple relationships can be connected in cascade to produce a single-phase seven-level inverter and eight power electronic switches are used. More recently, various novel topologies for seven-level inverters have been proposed. For example, a single-phase seven-level grid-connected inverter has been developed for a photovoltaic system [18]. This seven-level grid-connected inverter contains six power electronic switches. However, three DC capacitors are used to construct the three voltage levels, which results in that balancing the voltages of the capacitors is more complex. In [19], a seven-level inverter topology, configured by a level generation part and a polarity generation part, is proposed.

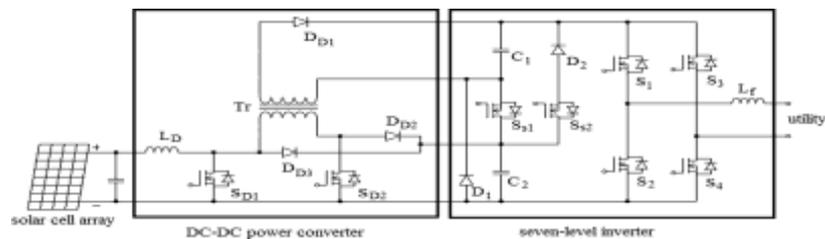


Figure 1. Configuration of The Existing Solar Power Generation System

There, only power electronic switches of the level generation part switch in high frequency, but ten power electronic switches and three DC capacitors are used. In [20], a modular multilevel inverter with a new modulation method is applied to the photovoltaic grid-connected generator. The modular multilevel inverter is similar to the cascade H-bridge type. For this, a new modulation method is proposed to achieve dynamic capacitor voltage balance. In [21], a multilevel DC-link inverter is presented to overcome the problem of partial shading of individual photovoltaic sources that are connected in series. The DC bus of a full-bridge inverter is configured by several individual DC blocks, where each DC block is composed of a solar cell, a power electronic switch, and a diode. Controlling the power electronics of the DC blocks will result in a multilevel DC-link voltage to supply a full-bridge inverter and to simultaneously overcome the problems of partial shading of individual photovoltaic sources. The above literature does not deal with boost SEPIC fed nine level inverter. This work proposes boost SEPIC converter between PV and inverter.

This paper proposes a new solar power generation system. The proposed solar power generation system is composed of a DC/DC power converter and a nine-level inverter. The nine-level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascade. The nine-level inverter contains only eight power electronic switches, which simplifies the circuit configuration.

2. CIRCUIT CONFIGURATION

Figure 1 shows the configuration of the existing solar power generation system. The proposed solar power generation system is composed of a solar cell array, a DC–DC power converter, and a new nine-level inverter. The solar cell array is connected to the DC–DC power converter, and the DC–DC power converter is a boost converter cascaded with SEPIC. The DC–DC power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the nine level inverter. This new nine-level inverter is bridge power converter, connected in a cascade. The power electronic switches of capacitor selection circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in series. Because of the multiple relationships

between the voltages of the DC capacitors, the capacitor selection circuit outputs a three-level DC voltage. The full-bridge power converter further converts this three-level DC voltage to a seven-level AC voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility, which produces a unity power factor.

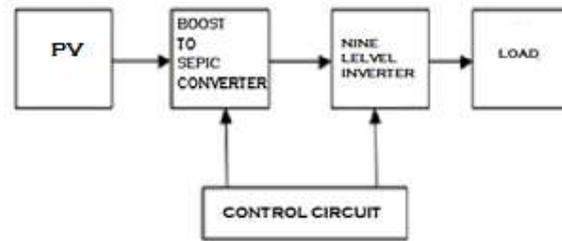


Figure 2. Block Diagram of Proposed System

3. SIMULATION RESULTS

The simulation is done using the elements of mat lab and the results are presented here. The BBCFMLI system with the R load is shown in the Figure 3.1. The output voltage of the solar system is 15v as shown in the Figure 3.2. The switching pulses for the boost converter are shown in the Figure 3.3. The output voltage of the SEPIC converter is shown in the Figure 3.4. The circuit of boost to SEPIC converter is shown in the Figure 3.5. The switching pulses for bridge 1 and bridge 2 are shown in Figure 3.6 and 3.7 respectively. Nine level output voltage and output current are shown in the Figure 3.8 and 3.9 respectively. Frequency spectrum is shown in the Figure 3.10. the THD is 15.03%.

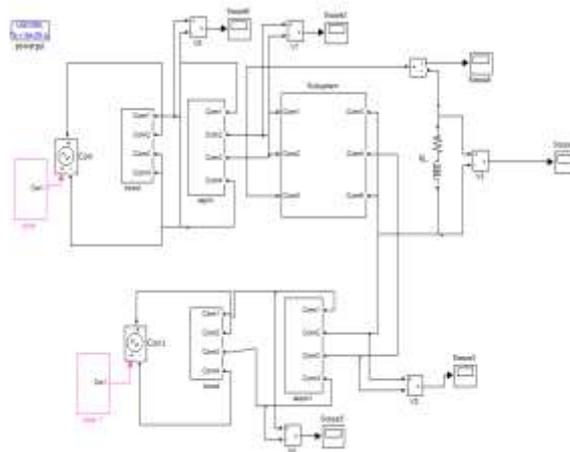


Figure 3.1. Circuit Diagram of Nine Level Inverter System with the RL Load

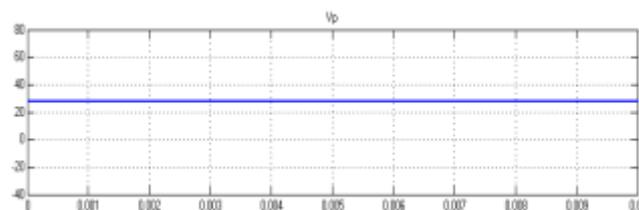


Figure 3.2. Output Voltage of the PV System

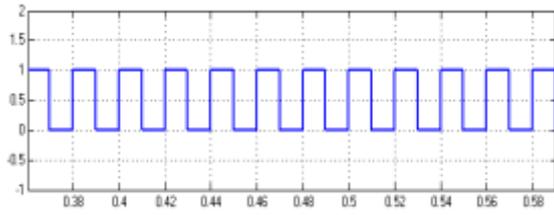


Figure 3.3. Switching Pulses for the Sepic Converter

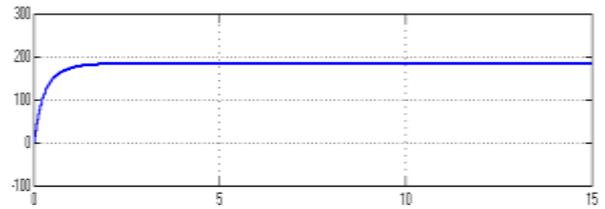


Figure 3.4. Output Voltage of the Boost to SEPIC Converter

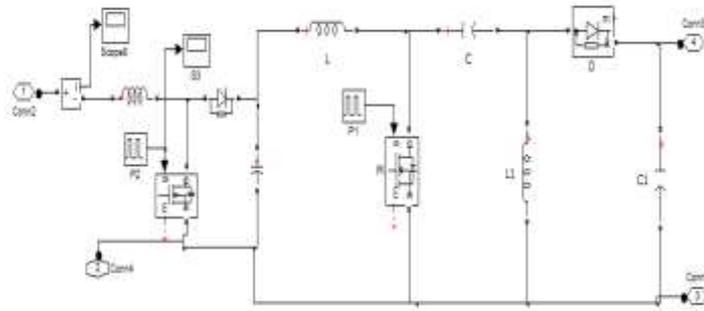


Figure 3.5. Boost to SEPIC Converter

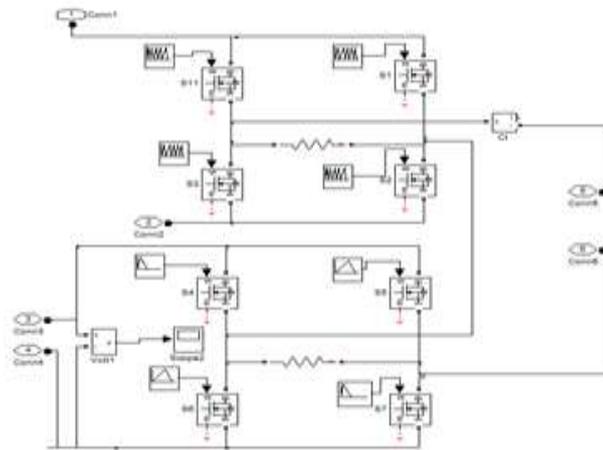


Figure 3.6. Nine Level Inverter

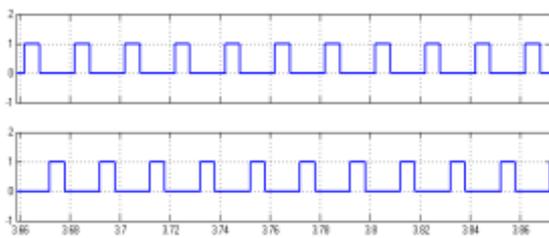


Figure 3.7. Switching Pulses for the H Bridge 1

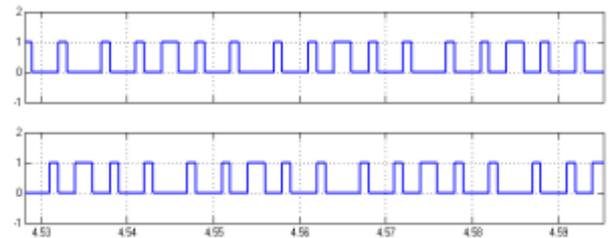


Figure 3.8. Switching Pulses for the H Bridge 2

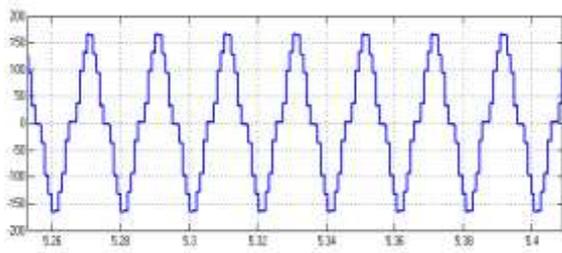


Figure 3.9. Output Voltage of the MLI

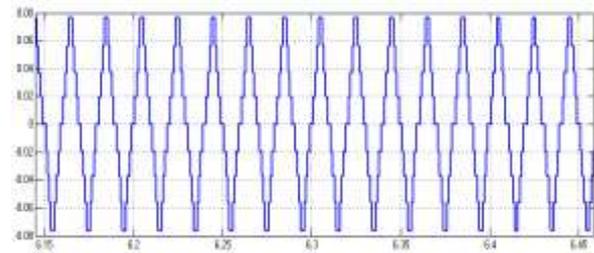


Figure 3.10. Output Current of the MLI

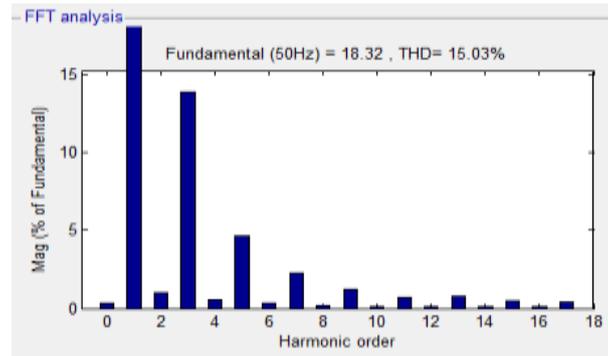


Figure 3.11. Frequency Spectrum for the Output Current

4. HARDWARE DETAILS

The hardware is engineered and tested in the laboratory. The hardware snap shot is shown in Figure 4.1. The output voltage of solar system is shown in Figure 4.2. The output voltage of stage 1 and stage 2 are shown in Figures 4.3 and 4.4 respectively. Switching pulse and driver output for M1 are shown in Figures 4.5 and 4.6 respectively. Switching pulse and driver output for M3 are shown in Figure 4.7 and 4.8 respectively. The output of MLI is shown in Figure 4.9.



Figure 4.1. Hardware Snap Shot



Figure 4.2. Solar Output Voltage



Figure 4.4. Output Voltage of Boost to SEPIC



Figure 4.5. Switching Pulse for M1, M3 of Inverter

converter

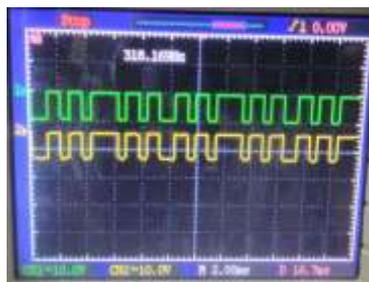


Figure 4.6. Driver Output Pulse for M1, M5



Figure 4.9. Output Voltage of MLI

5. CONCLUSION

The BBCFMLI System was designed, modelled and simulated successfully using Matlab. The simulation results indicate that the THD is reduced with RL load and induction motor load. The hardware is fabricated and tested in laboratory. The experimental results shown in Figure 4 matches with the simulation results shown in Figure 3. The advantages of this system are the reduction in the losses and reduction in heating of induction motor. The disadvantage of this system is that it requires two H-Bridges. This work deals with simulation of open loop control system. The closed loop system with various controllers will be investigated in future.

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